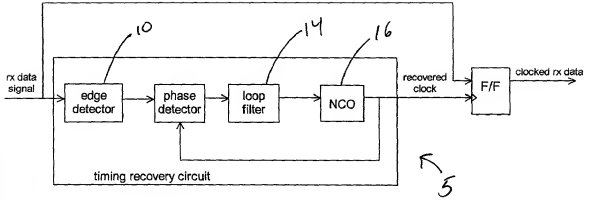

FIG 1. Timing recovery in a digital receiver. (PRIOR ART)

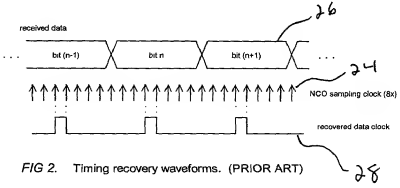

FIG 2. Timing recovery waveforms. (PRIOR ART)

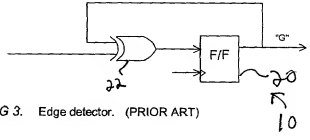

FIG 3. Edge detector. (PRIOR ART)

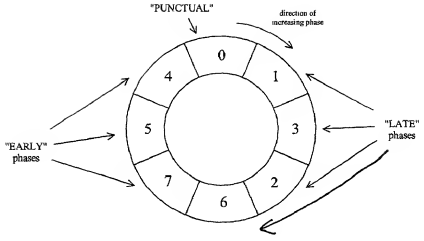

FIG 4. Nonlinear phase counter.

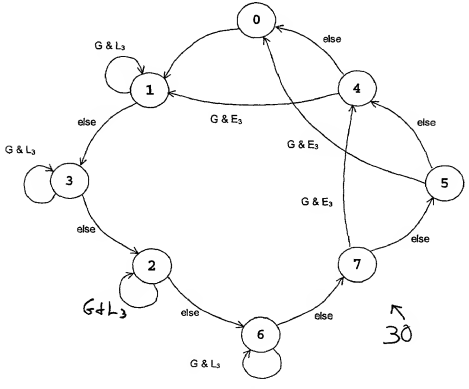

FIG 5. State machine "C", the phase counter.

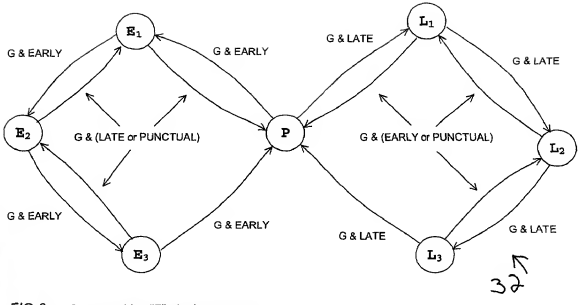

FIG 6. State machine "F", the loop counter.

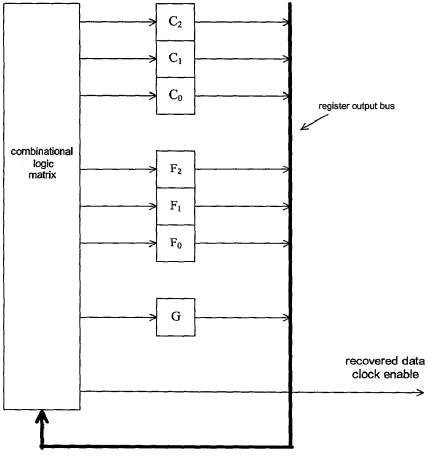

FIG 7. Logic circuit implementation of simplified timing recovery circuit.